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10/710,889	08/11/2004	Hui-Huang Chang	REAP0035USA	4888

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EXAMINER	
YU, HENRY W	
ART UNIT	**PAPER NUMBER**
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,889	CHANG, HUI-HUANG	
	Examiner	Art Unit	
	Henry Yu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/710,889.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/710,889 has a total of 18 claims pending in the application; there are 6 independent claim and 12 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING PRIORITY

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on October 8, 2003. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/710,889, filed on August 10, 2004.

II. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

III. INFORMATION CONCERNING DRAWINGS

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Item 12 in Fig. 1 is labeled as "*Control interface circuit*," while the written specification labels item 12 as "*interface control circuit*."

Item 70 in Fig. 4 is labeled as "*Data select sequence*," while the written specification labels item 70 as "*Data select sequence table*."

Item 73 in Fig. 6 is labeled with Chinese characters (instead of an English label), while the written specification labels item 70 as "*data selector*."

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

IV. OBJECTIONS TO THE SPECIFICATION

Specification

5. The disclosure is objected to because of the following informalities:

In **[paragraph 0007]**, the passage "*at last, the data can be outputted according to an output/input timing*" is awkwardly worded. Examiner suggests Applicant replace "*at last*" with –*finally* –.

In **[paragraph 0016]**, the passage "*a schematic diagram of an embodiment interface control circuit*" is awkwardly worded. Examiner suggests Applicant insert "*of*" between "*embodiment*" and "*interface.*"

In **[paragraph 0017]**, item 36 is referred to as "*control tables*" while earlier in the specification in **[paragraph 0016]** item 36 is referred to as "*control table.*" Examiner suggests Applicant use the same term when referring to item 36 throughout the specification.

In **[paragraph 0018]**, the passage "*please refer to Fig. 3, which is a detailed…*" is awkwardly worded. Examiner suggests Applicant replace the passage with –*Fig. 3 is a detailed…*–.

In **[paragraph 0018]**, item 64 is referred to as "*output/input timing control module*" and "*pin select sequence module,*" while the drawings refer to item 64 as "*output/input timing control module.*" Also, earlier in the specification in **[paragraph 0018]** "*pin select sequence module*" is referred to as item 62. Examiner suggests Applicant use the same term when referring to items 62 and 64 throughout the specification.

In **[paragraph 0020]**, the passage "*Refer to both Fig. 5 and Fig. 4*" is awkwardly worded. Examiner suggests Applicant replace the passage with –*Referring to both Fig. 5 and Fig. 4*–.

In **[paragraph 0021]**, the passage "*Please refer to Fig. 6, which shows…*" is awkwardly worded. Examiner suggests Applicant replace the passage with –*Fig. 6 shows…*–.

Appropriate correction is required.

V. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claim 11** is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The "*level data set*" as disclosed in lines 2-3 is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Since mention of the "*level data set*" is absent from the written specification, it is unclear what the element's intended function is or how the element relates to the rest of the invention. This ambiguity prevents proper enablement of this particular element of the claimed invention.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-2, 10, 12, 14, 16, and 18** are rejected under 35 U.S.C. 102(e) as being anticipated by Bacigalupo (Patent Number US 6,668,301 B2).

As per **claim 1**, Bacigalupo discloses "*an interface control circuit used in a circuit system for transmitting data, the interface control circuit comprising: a plurality of I/O pins*" as **[a semiconductor device is disclosed that has a plurality of I/O pins (Column 5, lines 3-4)]**. Bacigalupo also discloses "*an I/O-pin select sequence table for recording at least an I/O-pin data set*" as **[EBU (external bus interface unit)…selectively provides interface signals to the appropriate external device based on external device information…from the external device look-up table…that is based on at least some of the core signals…that are provided to EBU (Column 9, line 16-20)]**. Bacigalupo further discloses "*and an I/O-pin sequence select module for transmitting the data sequentially through the plurality of I/O pins according to the I/O-pin data set*" as **[the microcontroller…includes a plurality of data pins…for interfacing with corresponding data pins…of the external device. The microcontroller…may include any suitable number of data pins that are appropriate for interfacing with various external devices with different memory sizes (Column 9, lines 32-37)]**.

As per **claim 2**, Bacigalupo discloses "*the circuit system is coupled to a second circuit* system" as **[a microcontroller…coupled with a plurality of eternal devices (Column 7, lines 7-8)]**. Bacigalupo also discloses "*content of the I/O-pin select sequence table conforms to requirements of the second circuit system*" as **[the external device look-up table…may include external device information…for each set of**

core signals…that are associated with a particular external device (Column 8, lines 19-22)].

As per **claim 10**, Bacigalupo discloses "*an interface control circuit for outputting a timing signal, the interface control circuit comprising: a timing control table for providing a cycle data set, the cycle data set corresponding to the timing signal*" as **[the table…is programmable (e.g., by core signals…) and may be programmed to provide external device information for any suitable number of external device types that may be accommodated by the microcontroller's pins (Column 8, lines 42-46)]** and **[each of the information sets may include different timing parameters for the same type of external device or the same timing parameters (Column 8, lines 57-59)]**. Bacigalupo also discloses "*and a timing control unit for outputting the timing signal according to the cycle data set*" as **[the microcontroller may be designed to also selectively provide appropriately timed interface signals to external devices having the same type but having different interface signal timing requirements (Column 7, lines 36-39)]**.

As per **claim 12**, *see rejection to **claim 2** above*.

As per **claim 14**, *see rejection to **claim 1** above*.

As per **claim 16**, *see rejection to **claim 1** above*.

As per **claim 18**, Bacigalupo discloses "*a method for outputting a control signal comprising: determining an output/input timing according to an output/input timing control table*" as **[these microcontroller…pins are configurable to provide byte control and chip select functions to the external device (Column 9, lines 52-54)]**,

where **[EBU…selectively provides interface signals to the appropriate external device based on external device information…from the external device look-up table…(Column 9, lines 16-18)]**. There are different **[timing diagrams for I/O signals that are required as input into the external device…to enable write operation (Column 2, lines 18-20)]** and **[read operation (Column 2, lines 21-22)]** for various external devices **(Figs._1B, 1C, 2B, 2C, 3B, 3C, 4B, and 4C)**. Bacigalupo also discloses "*outputting the control signal according to the output/input timing*" as **[the microcontroller may be designed to also selectively provide appropriately timed interface signals to external devices (Column 7, lines 36-38)]**.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. **Claims 3-9, 11, 13, 15, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacigalupo (Patent Number US 6,668,301 B2) in view of Bell et al. (Patent Number US 6,038,400).

As per **claim 3**, Bacigalupo discloses "*the interface control circuit*" (*see rejection to **claim 1** above*). However, Bacigalupo does not disclose "*a data select sequence table for providing a predetermined sequence*" or "*a data sequence select module for sequentially transmitting the data according to the predetermined sequence through at least one of the I/O pins.*"

Bell et al. discloses "*a data select sequence table for providing a predetermined sequence*" as **[Protocol implementing circuitry…sends the data signal from DIN line…to shift register…(Column 7, lines 59-60)]**. Bell et al. also discloses "*a data sequence select module for sequentially transmitting the data according to the predetermined sequence through at least one of the I/O pins*" as **[the loaded data may then be shifted out one bit at a time on DOUT signal line…in synchronization with clock signals on CLK line…Thus the processor may read the data in register…by selecting integrated circuit…sending clock pulses to integrated circuit…and reading the bits on DOUT line (Column 8, lines 15-20)]**.

Bacigalupo and Bell et al. are analogous art because they are from the same field of adaptable bus interfacing with various protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the interface control circuit as disclosed by Bacigalupo to include a system that sequentially transmits data as disclosed by Bell et al.

The motivation for doing so would have been because Bell et al. teaches that **[to offer its customers a variety of interface options integrated circuit manufacturers must provide multiple versions of an integrated circuit design, each version supporting one of the interface protocols. This leads to a proliferation of integrated circuit devices having similar functionality, but each having a unique part number. Thus a customer must be familiar with the variations of each design and must purchase and inventory a large number of unique parts. Likewise, manufacturers must maintain an inventory of many unique parts, resulting in increased costs (Column 4, lines 14-23)]**. In order to streamline the number of components that service various protocols, one of ordinary skill in the art at the time of invention would create a single interface system that is capable of coupling with devices of various protocols automatically (whether it is through control, timing, or data signals), utilizing information stored within a table/register that the interface system can utilize.

As per **claim 4**, Bacigalupo discloses "*the interface control circuit*" (*see rejection to **claim 1** above*). Though Bacigalupo discloses "*a timing control table for providing a cycle data set*" as **[EDU…selectively provides interface signals to the appropriate external device based on external device information…from the external device look-up table…(Column 9, lines 16-18)]**, Bacigalupo does not explicitly disclose the timing portion of "*a timing control table for providing a cycle data set,*" nor does Bacigalupo disclose "*a timing control unit for transmitting the data according to the cycle data set.*"

Bell et al. explicitly discloses the timing portion of "*a timing control table for providing a cycle data set*" as **[the incrementing of register...may be performed in accordance with the principles of modulo arithmetic, so that when the value in register...reaches a maximum possible value, a subsequent CLK pulse causes the value in register...to "roll over" to a small value (Column 6, lines 50-54)]**. Bell et al. also discloses "*a timing control unit for transmitting the data according to the cycle data set*" as **[pulses provided on the CLK line synchronize the transfer of data from the processor to the target device (on the DIN line), or from the device to the processor (on the DOUT line) (Column 2, lines 8-11)]**.

Bacigalupo and Bell et al. are analogous art because they are from the same field of adaptable bus interfacing with various protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the interface control circuit as disclosed by Bacigalupo to include a variable timing system as disclosed by Bell et al.

The motivation for doing so would have been because Bacigalupo notes that **[although a particular microcontroller typically meets the interfacing requirements for one or two types of external device, conventional microcontrollers are typically not capable of interfacing with more than one type of external device (Column 4, lines 40-44)]**. Bell et al. expands on this by teaching that **[to offer its customers a variety of interface options integrated circuit manufacturers must provide multiple versions of an integrated circuit design, each version supporting one of the interface protocols. This leads to a**

proliferation of integrated circuit devices having similar functionality, but each having a unique part number. Thus a customer must be familiar with the variations of each design and must purchase and inventory a large number of unique parts. Likewise, manufacturers must maintain an inventory of many unique parts, resulting in increased costs (Column 4, lines 14-23)]. In order to streamline the number of components that service various protocols, one of ordinary skill in the art at the time of invention would create a single interface system that is capable of coupling with devices of various protocols automatically, including timing signals, utilizing information stored within a table/register that the interface system can utilize.

As per **claim 5**, Bacigalupo discloses "*the interface control circuit*" (*see rejection to **claim 1** above*). However, Bacigalupo does not disclose "*the timing control unit outputs a timing signal according to the cycle data set.*"

Bell et al. discloses "*the timing control unit outputs a timing signal according to the cycle data set*" as **[pulses provided on the CLK line synchronize the transfer of data from the processor to the target device…(Column 2, lines 8-9)]**.

Bacigalupo and Bell et al. are analogous art because they are from the same field of adaptable bus interfacing with various protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the interface control circuit as disclosed by Bacigalupo to include a variable timing system as disclosed by Bell et al.

The motivation for doing so would have been because Bacigalupo notes that **[although a particular microcontroller typically meets the interfacing requirements for one or two types of external device, conventional microcontrollers are typically not capable of interfacing with more than one type of external device (Column 4, lines 40-44)]**. Bell et al. expands on this by teaching that **[to offer its customers a variety of interface options integrated circuit manufacturers must provide multiple versions of an integrated circuit design, each version supporting one of the interface protocols. This leads to a proliferation of integrated circuit devices having similar functionality, but each having a unique part number. Thus a customer must be familiar with the variations of each design and must purchase and inventory a large number of unique parts. Likewise, manufacturers must maintain an inventory of many unique parts, resulting in increased costs (Column 4, lines 14-23)]**. In order to streamline the number of components that service various protocols, one of ordinary skill in the art at the time of invention would create a single interface system that is capable of coupling with devices of various protocols automatically, notably timing signals, utilizing information stored within a table/register that is accessible by the interface control system.

As per **claim 6**, Bacigalupo discloses "*an interface control circuit for transmitting data, the interface control circuit comprising: at least an I/O pin*" as **[a semiconductor device is disclosed that has a plurality of I/O pins (Column 5, lines 3-4)]**. However, Bacigalupo does not disclose "*a data select sequence table for providing a*

predetermined sequence" or "*a data sequence select module for sequentially transmitting the data according to the predetermined sequence through the I/O pin.*"

Bell et al. discloses "*a data select sequence table for providing a predetermined sequence*" as **[Protocol implementing circuitry…sends the data signal from DIN line…to shift register…(Column 7, lines 59-60)]**. Bell et al. also discloses "*a data sequence select module for sequentially transmitting the data according to the predetermined sequence through at least one of the I/O pins*" as **[the loaded data may then be shifted out one bit at a time on DOUT signal line…in synchronization with clock signals on CLK line…Thus the processor may read the data in register…by selecting integrated circuit…sending clock pulses to integrated circuit…and reading the bits on DOUT line (Column 8, lines 15-20)]**.

Bacigalupo and Bell et al. are analogous art because they are from the same field of adaptable bus interfacing with various protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the interface control circuit as disclosed by Bacigalupo to include a system that sequentially transmits data as disclosed by Bell et al.

The motivation for doing so would have been because Bell et al. teaches that **[to offer its customers a variety of interface options integrated circuit manufacturers must provide multiple versions of an integrated circuit design, each version supporting one of the interface protocols. This leads to a proliferation of integrated circuit devices having similar functionality, but each having a unique part number. Thus a customer must be familiar with the variations o each design**

and must purchase and inventory a large number of unique parts. Likewise, manufacturers must maintain an inventory of many unique parts, resulting in increased costs (Column 4, lines 14-23)]. In order to streamline the number of components that service various protocols, one of ordinary skill in the art at the time of invention would create a single interface system that is capable of coupling with devices of various protocols automatically (whether it is through control, timing, or data signals), utilizing information stored within a table/register that is accessible by the interface control system.

As per **claim 7**, the combination of Bacigalupo and Bell et al. discloses "*the interface control circuit*" (*see rejection to **claim 6** above*). Bacigalupo further discloses "*the circuit system is coupled to a second circuit* system" as **[a microcontroller…coupled with a plurality of eternal devices (Column 7, lines 7-8)]**. Bacigalupo also discloses "*content of the data select sequence table conforms to requirements of the second circuit system*" as **[the external device look-up table…may include external device information…for each set of core signals…that are associated with a particular external device (Column 8, lines 19-22)]**.

As per **claim 8**, *see rejection to **claim 4** above*.

As per **claim 9**, *see rejection to **claim 5** above*.

As per **claim 11**, Bacigalupo discloses "*the interface control circuit*" (*see rejection to **claim 10** above*). However, Bacigalupo does not disclose "*a level data set, and the level data set is related to the timing signal.*"

Bell et al. discloses "*a level data set, and the level data set is related to the timing signal*" as **[protocol implementing circuitry...sends the data signal from DIN line...to shift register...via DIN line...and in response to clocking pulses on the CLK line (Column 7, lines 59-61)]**.

Bacigalupo and Bell et al. are analogous art because they are from the same field of adaptable bus interfacing with various protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the interface control circuit as disclosed by Bacigalupo to include a system that has a data set relating to a timing signal as disclosed by Bell et al.

The motivation for doing so would have been because Bacigalupo notes that **[although a particular microcontroller typically meets the interfacing requirements for one or two types of external device, conventional microcontrollers are typically not capable of interfacing with more than one type of external device (Column 4, lines 40-44)]**. Bell et al. expands on this by teaching that **[to offer its customers a variety of interface options integrated circuit manufacturers must provide multiple versions of an integrated circuit design, each version supporting one of the interface protocols. This leads to a proliferation of integrated circuit devices having similar functionality, but each having a unique part number. Thus a customer must be familiar with the variations o each design and must purchase and inventory a large number of unique parts. Likewise, manufacturers must maintain an inventory of many unique parts, resulting in increased costs (Column 4, lines 14-23)]**. In order to

streamline the number of components that service various protocols, especially when it comes to the different timing specifications of various protocols, one of ordinary skill in the art at the time of invention would create a single interface system that is capable of coupling with devices of various protocols automatically.

As per **claim 13**, *see rejection to **claim 3** above*.

As per **claim 15**, *see rejection to **claim 4** above*.

As per **claim 17**, *see rejection to **claim 4** above*.

VII. RELEVENT ART CITED BY THE EXAMINER

13. The following prior art made of record and relied upon is citied to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c).**

14. The following references teach interfacing and connection of devices with various protocols:

U.S. PATENT NUMBERS:

4,222,103

5,701,514

5,727,170

6,026,453

6,038,400

6,088,754

6,138,177

6,668,301 B2

NON-PATENT LITERATURE:

Chung, Ki-Seok et al. "An Algorithm for Synthesis of System-Level Interface Circuits." *Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design.* January 1997.

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

15. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P 707.07(i):**

a(1). CLAIMS REJECTED IN THE APPLICATION

16. Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a first action non-final.

17. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

18. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Yu whose telephone number is (571) 272-9779. The examiner can normally be reached on Monday to Friday, 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pierre Vital can be reached on (571) 272-4215. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 4, 2007

Henry Yu
Art Unit 2112

PIERRE VITAL
SUPERVISORY PATENT EXAMINER